FACULTY OF INFORMATION TECHNLOGY

COMPUTER SYSTEMS ENGINEERING DEPARTMENT

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LAB (ENCS 211)

Report - Experiment VIII

VERILOG: PART II

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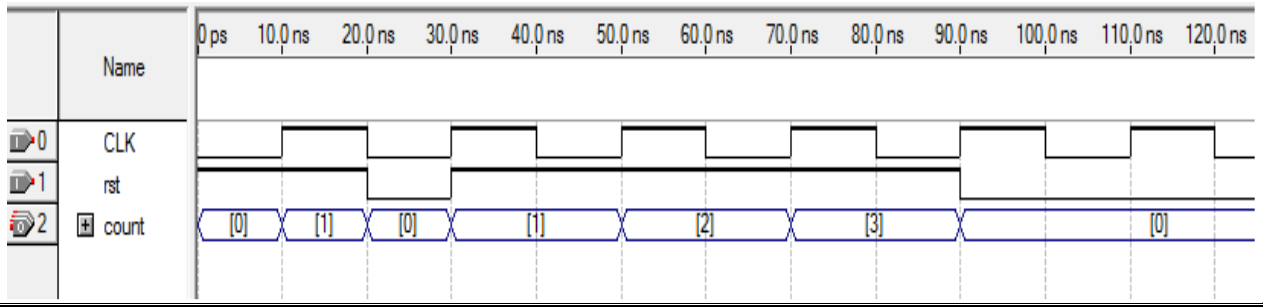
4-Bit Counter: The counter has two inputs; Clock (clk), Reset (rst) and one output (count).

Counter Project:

counter.v | Compilation Report - Flow Summary

```
1  module counter( clk , rst , count  );
2  input clk , rst ;
3  //declaring the inputs
4  output [3:0] count ;
5  //declaring the output
6  reg [3:0] count ;
7  always @ (posedge clk or negedge rst )
8  if (~rst)
9  count = 4'b0000;
10 else
11 count = count + 1 ;
12 // keep adding 1 to count unless reset  = 0
13 endmodule
14 //ending the module !
```

Functional Simulation:



Default Symbol: